Versatile Computing Systems

VCompS-1000 Custom System on Chip (cSoC)

Complete Processing and Networking Solution Optimized for Space, Weight, Power, Obsolescence, and Total System Effectiveness

Flexible Dual Computing Solution

- High-integrity lockstep processors <or>
- Two fully independent processors in one package
- Less than eight watts with all features enabled

High Performance Avionics Networking

- High-integrity I/O using built-in ARINC 664 End Systems <or>
- Dedicated network processing lanes as a standalone or integrated solution
- Market-leading network performance

Versatile Open Systems Empower the System Integrator

- Based on industry-standard open systems and built to empower the aircraft system integrator with control over all aspects of the system
- Create a variety of scalable avionics solutions using compatible building blocks from our Versatile Computing product family

Beat Obsolescence From Day One

- Preserve technology for the lifetime of the avionics solution
- Dedicated long-term support and manufacture of the device
- Ownership of intellectual property enables fabrication for years to come

Efficient Full-System Approach

- Full artifacts to efficiently create safe, certifiable systems at the highest levels of criticality
- Available as single device, 3U VPX mezzanine, or as a baseboard with varying I/O capabilities and form factors
- Same proven technology implemented in several of our innovative avionics solutions

geaviation.com
**Performance specifications**

**Processor Core**
- 1.2 GHz e5501 Power Architecture
- 32 KB Data and Instruction cache
- 256 KB L2 cache
- 256 KB L3 cache
- DDR4-1600 MHz controller, 64-bit data, 8-bit ECC and built-in DDR PHY

**Cross Lane Checking Features**
- Dual Lane Design: Lockstep or Independent Modes
- >1400 cross-lane checking signals
- Fully coordinated cross-lane lockstep JTAG debugging
- Cross-lane communication mailbox (not available in lock-step mode)

**Memory Interface**
- DDR and Flash Controllers
- NAND control /w ECC and built-in PHY
- Internal 512 KB Scratchpad SRAM /w ECC
- Internal ROM Boot loader
- Parallel bus for external memory interface, 32-bit data and 29-bit address

**Input/Output**
- ARINC 664 Part 7 (2x) <or>
  10/100/1000 Ethernet (2x)
- DDR4-2400 MHz I/O memory controller port, 64-bit data, 8-bit ECC and built-in DDR PHY
- Gen 3 PCIe w/ built-in PHY (x4 lane)
- SPI (1x)
- I2C (2x)
- UART (3x)
- GPIO (32x)

**Supporting Data and Information**
- DO-254 DAL A Certification Artifacts
- Production Specification

**Also Available**

**VCompS-1001 cSoC Development Environment (CDE)**
- Software application development environment
- Reference Design Board with full I/O breakout and Linux OS
- Debug Utilities
- Hardware Design Guide, Checklists, and Device Errata

**Additional Hardware Features**
- Interrupt Controller
- Internal DMA/Hash Engine (4x)
- GP Timers
- Windowed WDT
- Alternate Boot Manager
- Reset Control
- Temperature Sensors (5x)
- Power Isolation by Lane
- Embedded One-Time Programmable ROM
- Thermal and Voltage sensors
- Die Crack Detect
- Ball & Bump Integrity Detect
- Block Protection Units
- Peripheral Access Management Unit

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**Feature**

<table>
<thead>
<tr>
<th>Attribute</th>
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<tbody>
<tr>
<td>Power</td>
<td>&lt; 8 W</td>
</tr>
<tr>
<td>Size</td>
<td>31 mm X 31 mm (package)</td>
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**Operating Environment**

-40°C to +125°C (T)